ABSTRACT OF THE DISCLOSURE

An apparatus for testing a semiconductor die and the method wherein there is provided a package having a cavity therein with a plurality of terminals in the package disposed at the periphery of the cavity. A semiconductor die to be tested and having a plurality of bond pads thereon is disposed in the cavity and an interconnecting layer having electrically conductive paths thereon is also disposed in the cavity, each of the paths having first and second spaced apart regions thereon, the first region of each path being aligned with and contacting a bond pad. An interconnection is provided between the second spaced apart region of each of the paths and one of the plurality of terminals. The second spaced apart region of each of the paths is preferably a bump aligned with and contacting one of the plurality of terminals. A compliant layer is preferably disposed over the interconnecting layer and provides a force causing engagement of at least the first spaced apart regions and the bond pads. The first region is preferably a compliant bump probe tip having a first predetermined height above the layer and includes a standoff on the layer having a second predetermined height above the layer less than the first height.